GAU 1107

PATENT
Attorney Docket No.2718US(95-0837)

CERTIFICATE OF MAILING (under 37 C.F.R. § 1.10 if checked)

I hereby certify that this transmittal along with all items checked below is being deposited with the United States Postal Service

☐ as first class mail, postage prepaid (37 C.F.R. § 1.8)
☒ "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10
Express mail label mailing number: EM339601534US

on the date inserted below and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Timothy Ricks	December 10, 1997	
Typed name of person mailing transmittal	Date of Deposit	Signature of person mailing transmittal

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Serial No.:	08/602,503	Group Art Unit No.:	1107
Filing date:	February 20, 1996	Examiner:	K. Turner
For (title):	FLIP CHIP AND CONVENTIONAL STACK		

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION — 37 C.F.R. § 192)

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on October 14, 1997.

2. STATUS OF APPLICATION
This application is on behalf of
☒ other than a small entity
☐ small entity
verified statement:
☐ attached
☐ already filed

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 C.F.R. § 1.17(f) the fee for filing the Appeal Brief is:

☐	small entity status	$155
☒	other than a small entity	$310

4. EXTENSION OF TIME

☐ A petition for Extension of Time for a month extension of time for filing the Appeal Brief is enclosed.

5. FEE PAYMENT

☒ Check No. 09134 is enclosed in payment of the fee for filing the Appeal Brief plus any extension of time for which a petition has been filed.

☐ Please charge this fee to deposit account No. 20-1469 (a duplicate copy of this notice is enclosed--see below).

Any additional appeal fees which are not otherwise submitted herewith or which are insufficient should be charged to deposit account no. 20-1469. A duplicate copy of this notice is enclosed. Please address all communications in connection with this appeal to the address indicated below.

Respectfully submitted,

Robert G. Winkle
Reg. No. 37,474
TRASK, BRITT & ROSSA
P.O. Box 2550
Salt Lake City, UT 84110-2550
(801) 532-1922

Enclosures: As identified above
N:\2269\2718\APPBRIEF.TRN 12/10/97

1107 1933
#12 Appeal Brief
12-22-97
M. Ross

PATENT

12/10/97
JC540 U.S. PTO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Michael B. Ball

Serial No.: 08/602,503

Filed: February 20, 1996

For: FLIP CHIP AND CONVENTIONAL STACK

Examiner: K. Turner

Group Art Unit: 1107

Attorney Docket No.: 2718US (95-0837)

CERTIFICATE OF MAILING UNDER RULE 1.10

I hereby certify that this paper or fee along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service (under 37 C.F.R. § 1.10) (Express Mail Mailing Label Number: EM339601534US on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

12.10.97
Date of Deposit

Signature of person actually making deposit pursuant to 37 C.F.R. § 1.10(b)

Timothy Ricks
Typed/printed name of person whose signature is contained above

RECEIVED
DEC 18 1997

BRIEF ON APPEAL

Assistant Commissioner for Patents
Washington, D.C. 20231

Attention: Board of Patent Appeals and Interferences

Sirs:

This brief is submitted in the format of 37 C.F.R. § 1.192(c):

(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is the Micron Technology, Inc., assignee of the pending application as recorded with the United States Patent and Trademark Office on February 20, 1996, Reel 7879, Frame 0924.

(2) RELATED APPEALS AND INTERFERENCES

Neither the appellant, the appellant's representative nor the assignee is aware of any pending appeal or interference which would directly affect, be directly affected by or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF THE CLAIMS

Claims 19, 21-23, and 25-34 stand rejected.

Claims 1-18, 20, and 24 are canceled without prejudice.

No claims are allowed.

The rejections of claims 19, 21-23, and 25-34 are being appealed.

(4) STATUS OF AMENDMENTS

An Amendment After Final Rejection (pursuant 37 C.F.R. § 1.116) was filed on September 4, 1997 subsequent to the final rejection. The Amendment After Final Rejection included an analysis of the rejections to overcome the Examiner's rejections raised under 35 U.S.C. § 103. An Advisory Action mailed September 18, 1997 advised that the Amendment After Final Rejection would be entered upon the filing of an appeal, but the Section 103 rejections were not overcome. The Notice of Appeal was filed on October 13, 1997.

(5) SUMMARY OF THE INVENTION

The invention claimed in pending claims 19, 21-23, and 25-34 relates to a method of increasing integrated circuit density by stacking semiconductor dice and components (specification, page 6, lines 10 - et seq.). The method comprises supplying a substrate which has a plurality of conductors, a base die which is attached face down to the substrate to make electrical communication with at least some of the conductors, securing the back side of at least one active face-up stack die to the base die, electrically connecting the stack die to at least one of the conductors on the substrate, securing at least one discrete component to either the stack die, the base die, or the substrate, and electrically connecting the discrete component to the stack die, the base die, and/or the substrate (specification, page 6, lines 20 - et seq.). An example of this stacked configuration, with the discrete component attached to the base die and in electrical communication with the stack die and substrate, is represented in illustration 1:

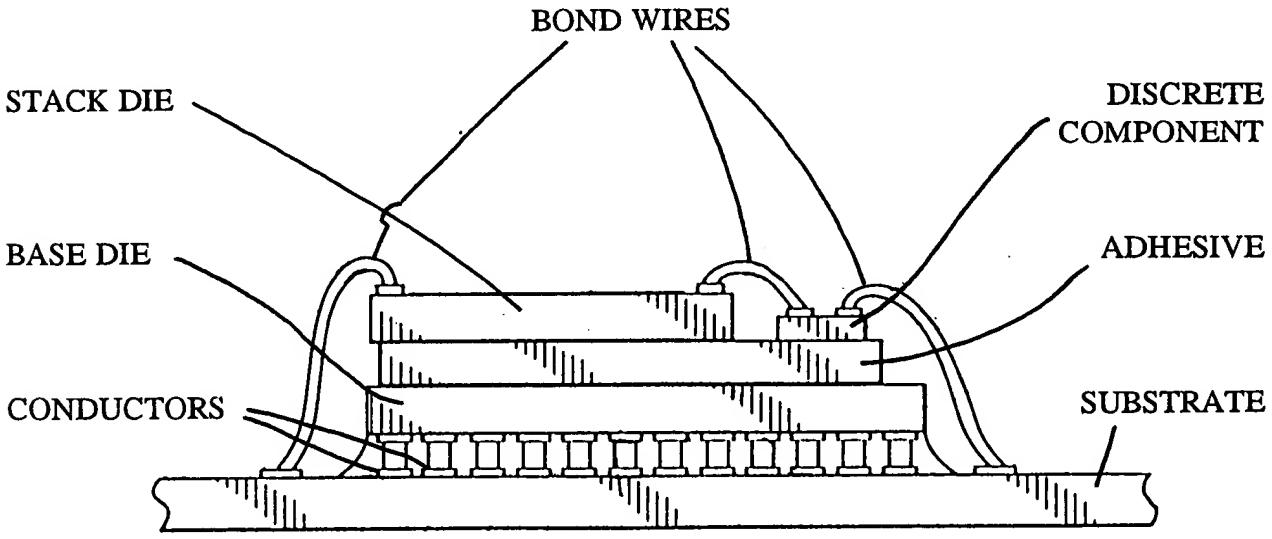


ILLUSTRATION 1

Although Illustration 1 shows bond wire connections between the stack die, the discrete component, and the substrate, the electrical connections can be achieved with TAB technology, wherein metal tape leads are attached between bond pads on the stack die and leads on the substrate. Thus, the present invention allows for increasing semiconductor device density using non-customized die and bond pad patterns, and commercially-practiced conductor attachment techniques.

The present invention is, of course, not limited to the example shown in Illustration 1. For example, additional dice and discrete components can be added to the arrangement in Illustration 1. As another example, and not by way of limitation, a pair of base dice can be connected to the substrate with the stack die bridged between the base dice pair with at least one discrete component secured to either the stack die, either of the base dice pair, or the substrate. Furthermore, still more additional dice can be stacked or discrete components attached to the assembly in the manner discussed above.

(6) ISSUES

A. Whether claims 19, 21-23, 25-29 and 33 are unpatentable under 35 U.S.C. § 103 over the Japanese Reference 63-179537 published July 23, 1988 attributed to Kuroda ("Kuroda") and Japanese Reference 63-104343 published May 9, 1988 attributed to Kuranaga ("Kuranaga") in view of U.S. Patent 5,323,060 issued June 21, 1994 to Fogal et al. ("Fogal")?

B. Whether claims 30-32 and 34 are unpatentable under 35 U.S.C. § 103 over Kuranaga and Kuroda in view of Fogal et al. (as applied to claims 19, 21-23, 25-29 and 33)

and further in view of U.S. Patent 5,399,898 issued March 21, 1995 to Rostoker ("Rostoker") and U.S. Patent 5,422,435 issued June 6, 1995 to Takiar et al. ("Takiar")?

(7) GROUPING OF CLAIMS

The grouping of the claims is as follows:

(a) Claim 19 recites a method for fabricating a multi-die assembly comprising providing a substrate including a plurality of conductors; attaching at least one active face-down base die to said substrate in electrical communication with at least some of said conductors; securing the back side of at least one active face-up stack die to said base die; electrically connecting said stack die to at least one of said conductors; securing at least one discrete component to at least one of said stack die, said base die, and said substrate; and electrically connecting said at least one discrete component to at least one of said stack die, said base die, and said substrate.

(b) Claims 21-23 and 25-34 stand with claim 19 and would fall with claim 19.

(8) ARGUMENT

(i.) 35 U.S.C. § 112, first paragraph

There are no rejections or issues under 35 U.S.C. § 112, first paragraph.

(ii.) 35 U.S.C. § 112, second paragraph

There are no rejections or issues under 35 U.S.C. § 112, second paragraph.

(iii.) 35 U.S.C. § 102

There are no rejections or issues under 35 U.S.C. § 102.

(iv.) 35 U.S.C. § 103

Kuroda and Kuranga in view of Fogal

The rejection of claims 19, 21-23, 25-29 and 33 under 35 U.S.C. § 103 over Kuroda and Kuranga in view of Fogal is improper and traversed. It is not apparent whether Kuroda and Kuranaga are each employed separately as primary references due to the use of the word "and", or are somehow to be combined with each other and with Fogal. The Examiner has not been clear on this point. Even the September 18, 1997 Advisory Action is unclear whether they are to be combined or not with the statement "the Kuranaga and Kuroda references could be taken together" at page 2.

Nonetheless, Kuranaga teaches connecting two chip pairs together. A first set of chips (i.e., chips 1a and 1b) are defined as "[t]he stacked chips of lower stage". A second set of chips (i.e., chips 2a and 2b) are defined as "the stacked chips of upper stage." If one were to glean a method from the five sentences of the constitution portion of the abstract, it would appear that the first set of chips is connected together, followed by connecting the second set of chips together. Lastly, the first set is connected to the second set with "wirings".

Aside from the deficiencies in Kuranaga admitted in the July 9, 1997 Final Official Action for failing to teach a "direct connection between the third chip and the substrate" and for failing to teach the use of discrete components in the assembly, Kuranaga also does not teach attaching a first chip to a substrate, then attaching a second chip to first chip. The July 9, 1997 Final Official Action stated that "chip 1a can be considered another substrate".

The question remains, why should chip 1a be considered another substrate (as defined by Applicant in the present application's specification at page 6, lines 12-14)? As asserted in the Applicant's response to the Final Official Action, there is no apparent suggestion that the Kuranaga chip 1a is interchangeable with a printed circuit board or leadframe. The reality is that Kuranaga does not teach or suggest the use of a substrate. In response to this point, the September 18, 1997 Advisory Action stated that "*with reference to Kurunaga, 'chip 1a can be considered another substrate.' The statement was made merely to show how the Kuranaga and Kuroda references could be taken together.*" However, this statement raises more questions than it answers. For example, how does this statement "show how the Kuranaga and Kuroda references could be taken together"? What is meant by "could be taken together"? The rejection states that the claims are obvious over Kuroda and Kuranaga in view of Fogal, so the question remains, is the Kuranaga reference required for the rejection or not, in light of the phrase "could be taken together"?

With regard to the combination of Kuranaga and Kuroda references, the July 9, 1997 Final Official Action at page 2 admits that "Kuranaga and Kuroda fail to teach a direct connection between the third chip and the substrate and fail to specifically illustrate discrete components." The Official Action attempts to overcome these deficiencies by combining these references with Fogal. Fogal teaches attaching discrete components to a stacked assembly, but fails to teach a chip mounted face down to the substrate with a chip mounted face up to the face down chip. In fact, Fogal teaches away from mounting chips face down to the substrate, since Fogal only teaches wire bonding for electrical communication for all of the

semiconductor dice rather than at least one flip-chip type attachment. In emphasis of this point, the Background of the Invention of the Fogal patent (column 1, lines 35-39), Fogal specifically mentions TAB, flip-TAB, and flip-chip attachment, but Fogal rejects these attachment techniques in favor of the wire bonding and stacking technique, as disclosed in Fogal.

In response to Applicant pointing out these deficiencies, the September 18, 1997 Advisory Action at page 2 appears to take the position that in order to teach away from a combination of references, the reference must preclude other embodiments ("[t]he Fogal reference is not precluding the use of flip-chip, TAB, flip-TAB, etc. with the disclosed stacking arrangement."). This is an inappropriate standard. A reference need not preclude all other combinations in order to teach away from such combinations. As set forth in In re Gurley, 31 USPQ2d 1130 (Fed. Cir. 1994), "[t]he degree of teaching away will, of course, depend on the particular facts; in general, a reference will teach away if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant." This is exactly the Applicant's point. The line of development taught in Fogal would not be productive of the present invention, because Fogal knew of alternate attachment techniques, but, nonetheless, pursued a line of development including only back-binding semiconductor chips to a substrate and using wire bonds for electrical communication. Thus, the "line of development flowing from" the Fogal reference is away from the present invention.

Furthermore, the July 9, 1997 Final Official Action at page 4 stated, with regard to this point which was raised in the Applicant's Amendment filed April 15, 1997 in response to the January 15, 1997 Official Action, that the "inventors intended use, while important, is not controlling of the use that one of ordinary skill in the art would have found obvious . . . ." The Applicant is somewhat confounded as to what the "intended use" of the device disclosed in the present invention has to do with teaching or suggestion for an obviousness rejection. The point is not what the "intended use" of the device is, but whether Fogal can be properly combined with Kuranaga and Kuroda. It cannot, because it teaches away from the attempted combination. "A reference should be considered as a whole, and portions arguing against or **teaching away from the claimed invention must be considered.**" (Emphasis added) Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 230 USPQ 416 (Fed. Cir. 1986).

Moreover, Kuranaga and Kuroda were published long prior to the filing of the Fogal application. Thus, there could not have been any teaching, suggestion, or motivation within either Kuranaga or Kuroda to include structures as disclosed by Fogal, and Fogal did not exist at that time. Alternately, if the rejection is taken in the order of Fogal in view of Kuranaga and Kuroda, Fogal would have had the teachings of Kuranaga and Kuroda available as prior art. However, Fogal specifically elected not to incorporate the teachings of either Kuranaga or Kuroda to develop a fabrication method as claimed in the present application, but instead relied upon a wire bond only method. Again, as discussed above, Fogal specifically mentions TAB, flip-TAB, and flip-chip attachment, but nonetheless rejects use of these attachment techniques for the wire bonding and stacking technique disclosed. Thus, the only suggestion or

motivation for the combination of references as applied in the Official Action is Applicant's own specification, which constitutes an impermissible hindsight rejection, further explained below.

Furthermore, the *prima facie* case of obviousness has not been established. The M.P.E.P. 706.02(j) sets forth that:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. **The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.** *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The Examiner has the burden of establishing obviousness, yet has shown no teaching, suggestion, or incentive within Kuranaga, Kuroda, or Fogal et al. to combine these references. Thus, the references cannot properly be combined to reject claims 19, 21-23, 25-29 and 33 as obvious under Section 103(a).

For the foregoing reasons, neither Kuranaga, Kuroda, nor Fogal, alone or in any valid combination, teach or suggest that which is claimed and, therefore, do not render claims 19, 21-23, 25-29, and 33 obvious.

Kuroda and Kuranga in view of Fogal and further in view of Rostoker and Takiar

The rejection of claims 30-32 and 34 under 35 U.S.C. § 103 over Kuroda and Kuranga in view of Fogal and further in view of Rostoker and Takiar is improper and traversed.

The reasoning set forth above in response to the Section 103 rejection of claims 19, 21-23, 25-29 and 33 over Kuroda and Kuranaga in view of Fogal also applies to the present

rejection of claims 30-32 and 34 and is, therefore, incorporated by reference as though it had been repeated in total.

As discussed in the rejection of claims 19, 21-23, 25-29 and 33, neither Kuroda, Kuranaga, nor Fogal provide any teaching, suggestion, or motivation for their attempted combination. Furthermore, neither Rostoker nor Takiar et al. provide any teaching, suggestion, or motivation to combine any of the references in any combination. Rostoker relates only to bridging with flip-chip assemblies. Takiar et al. relates only to bridging wire bonded assemblies. There is no motivation to combine the references with regard to bridging two laterally adjacent face-down chips with one face-up chip to be wire bonded.

Assuming that the Fogal reference could be properly used as a reference (Applicant does not admit that it can be), the only way one might find that the bits and pieces from prior art suggests the present invention is with impermissible hindsight from the present application. There must be some teaching, suggestion or motivation in the art, and not in Applicants' disclosure, supporting the Examiner's combination of documents. See In re Fine, 5 U.S.P.Q.2d 1596, 1599-1600 (Fed. Cir. 1988) ("One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention"); Uniroyal v. Rudkin-Wiley, 5 U.S.P.Q.2d 1434, 1438 (Fed. Cir. 1988) (something in prior art as a whole must suggest desirability of combination). Both the suggestion to make the claimed combination and a reasonable expectation of success must be founded in the prior art, not in applicant's disclosure. In re Vaeck, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991).

Oddly, when presented with this current case law from the Federal Circuit, the Advisory Action retreats to a case which is over thirty years old and from a court that no longer exists to support the statement at page 4 "all of the references would considered [sic], as they all fall within field of endeavor of an ordinary skilled artisan in the packaging of semiconductor devices." Unfortunately, this statement is not the standard for showing why this is not a hindsight reconstruction. Again, there must be both the suggestion to make the claimed combination and a reasonable expectation of success must be founded in the prior art,

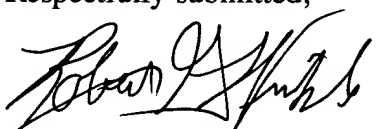
not in applicant's disclosure. Id. However, there has been no showing of teaching or suggestion in any of the five references to combine the bits and pieces together to render claims 30-32 and 34 obvious.

For the foregoing reasons, neither Kuranaga, Kuroda, Fogal, Rostoker nor Takiar alone or in any valid combination, teach or suggest that which is claimed and, therefore, do not render claims 30-32 and 34 obvious.

(9) APPENDIX

A copy of claims 19, 21-23, and 25-34 is appended hereto as "Appendix A."

Respectfully submitted,



Robert G. Winkle
Registration No. 37,474
Attorney for Applicants
TRASK, BRITT & ROSSA
P. O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: (801) 532-1922

Date: December 10, 1997

APPENDIX A

19. A method of fabricating a multi-die assembly, comprising:

providing a substrate including a plurality of conductors;

attaching at least one active face-down base die to said substrate in electrical communication with at least some of said conductors;

securing the back side of at least one active face-up stack die to said base die;

electrically connecting said stack die to at least one of said conductors;

securing at least one discrete component to at least one of said stack die, said base die, and said substrate; and

electrically connecting said at least one discrete component to at least one of said stack die, said base die, and said substrate.

21. The method of claim 19, further comprising:

extending a die-to-component bond wire between said at least one stack die and said at least one discrete component.

22. The method of claim 19, further comprising:

extending a component-to-substrate bond wire between said at least one discrete component and at least one of said plurality of substrate conductors.

23. The method of claim 19, further comprising:

securing a second stack die to said assembly; and

electrically connecting said second stack die and at least one of said plurality of substrate conductors.

25. The method of claim 23, further comprising securing said second stack die to said stack die.

26. The method of claim 25, further comprising:

securing at least one discrete component to said stack die; and

extending a die-to-component bond wire between said second stack die and said at least one discrete component.

27. The method of claim 25, further comprising:

securing at least one discrete component to said stack die; and

extending a component-to-substrate bond wire between said at least one discrete component and at least one of said plurality of substrate conductors.

28. The method of claim 25, further comprising:

securing at least one discrete component to said base die; and

extending a die-to-component bond wire between said second stack die and said at least one discrete component.

29. The method of claim 25, further comprising:

securing at least one discrete component to said base die; and

extending a component-to-substrate bond wire between said at least one discrete component and at least one of said plurality of substrate conductors.

30. The method of claim 19, further comprising attaching a second active face-down base die to said substrate in electrical communication with at least one of said plurality of substrate conductors.

31. The method of claim 30, further comprising bridging said stack die between said base die and second base die.

32. The method of claim 31, further comprising securing a second stack die over said stack die.

33. The method of claim 19, further comprising:

securing at least one discrete component to said substrate; and

extending a die-to-component bond wire between said at least one stack die and said at least one discrete component.

34. The method of claim 31, further comprising:

securing at least one discrete component to said substrate; and

extending a die-to-component bond wire between said at least one stack die and said at least one discrete component.